Design of a Low Power Flip-Flop Using MTCMOS Technique

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ABSTRACT

This paper enumerates low power, high speed design of Flip-Flops having less number of transistors and only one transistor being clocked by short pulse train which is true single phase clocking (TSPC) Flip-Flop. As transistors used have small area and low power consumption, they can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The Flip-Flops are analyzed at 90nm, 70nm and 50nm technologies. As the technology is scaled down, the leakage power increases, which is reduced by using MTCMOS technique. The designed Flip-Flops and Latches are compared in terms of power consumption, propagation delays and power dissipation product using DSCH and Microwind tools.

Keywords

CMOS, figure of merit, leakage current, power, delay, TSPC flip-flop.

1. INTRODUCTION

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data[1]. At each rising or falling edge of a clock signal, the data stored in a set of Flip-Flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered Flip-Flops otherwise it is called as single edge triggered Flip-Flops.

In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation [4][5]. Furthermore, the leakage power also becomes highly significant. High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced[6][7][8]. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power especially for High-speed and low-power applications. Multithreshold Voltage Based CMOS (MTCMOS) and voltage scaling are two of the low power techniques used to reduce power.

When technology scales down, total power dissipation will decrease and at the same time delay varies depends upon supply voltage, threshold voltage, aspect ratio, oxide thickness, load capacitance. CMOS devices have scaled downward aggressively in each technology generation to achieve higher integration density and performance. In this paper, the D Flip-Flop is designed and verified using MTCMOS technique.

The paper is organized as the discussion on previous technique in section-II. Section-III gives the details about the proposed MTCMOS based D-Flip Flop and its functionality. Section-IV gives details about the simulation results and comparison. Section-V concludes the paper.

TSPC FLIP FLOPS

In literature, many techniques are proposed for latches and Flip-Flops. The traditional CMOS based Flip-Flop uses 8 transistors[1]. Later a Latch was developed using 6 transistors where 4 NMOS transistors and 2 PMOS transistors are used for the design[1][2][3]. The schematic of TSPC flip-flop is shown in Fig. 1. This flip-flop is built using 3 NMOS transistors and 2 PMOS transistors [1][2][3].

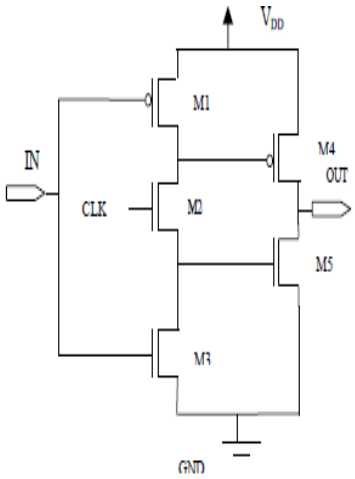

Fig. 1.TSPCflip-flop

Fig. 1 shows positive edge triggered 5 Transistor D latch. When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the values of input it becomes output. It also acts as a Flip-Flop when the input IN has less pulse width. Table.1 describes the truth table of TSPC D-Flip Flop in brief.

Table.1: Truth Table of D-Flip-Flop

CLK	IN	M1	M2	M3	M4	M5	OUT
↑	0	ON	ON	OFF	OFF	ON	0
↑	1	OFF	ON	ON	ON	OFF	1
↓	0	ON	OFF	OFF	OFF	OFF	0
↓	1	OFF	OFF	ON	OFF	OFF	0

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2. MTCMOS BASED D FLIP FLOP

MTCMOS is one of the most important low power technique which effectively reduces the leakage power. The MTCMOS operates in two modes – high threshold and low threshold modes. The high threshold mode reduces the leakage power and low threshold mode improves the speed performance. Fig. 2 shows TSPC D Flip-Flop designed with this technique.

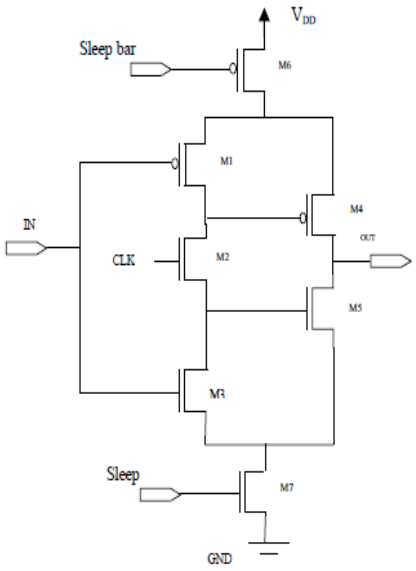

Fig. 2.MTCMOS flip-flop

To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are operated with high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal Mode. Table.2 describes the MTCMOS based D Flip-Flop in brief.

Table.2 MTCMOS based D Flip-Flop

CLK	IN	Sleep	M1	M2	M3	M4	M5	M6	M7	OUT
↑	0	0	ON	ON	OFF	OFF	ON	ON	OFF	0
↑	0	1	ON	ON	OFF	OFF	OFF	OFF	ON	0
↑	1	0	OFF	ON	ON	ON	OFF	ON	OFF	1
↑	1	1	OFF	ON	ON	ON	OFF	OFF	ON	1
↓	0	0	ON	OFF	OFF	OFF	OFF	ON	OFF	0
↓	0	1	ON	OFF	OFF	OFF	OFF	OFF	ON	0
↓	1	0	OFF	OFF	ON	OFF	OFF	ON	OFF	0
↓	1	1	OFF	OFF	ON	ON	OFF	OFF	ON	0

3. RESULTS AND DISCUSSIONS

Performance analysis of Various Flip-Flops and latches is presented in this section. DSCH and MICROWIND Tools[9] are used to carry out the work for different technologies like 90nm, 70nm and 50nm.

The design of Schematics and layout for fig.1 and fig.2 are shown below. Fig.3 shows the simulated waveforms of TSPC based D Flip-Flop designed for 90nm and the corresponding layout is shown in fig.4. Fig.5 shows the simulated waveforms of MTCMOS based D Flip-Flop designed for 90nm and the corresponding layout is shown in fig.6.

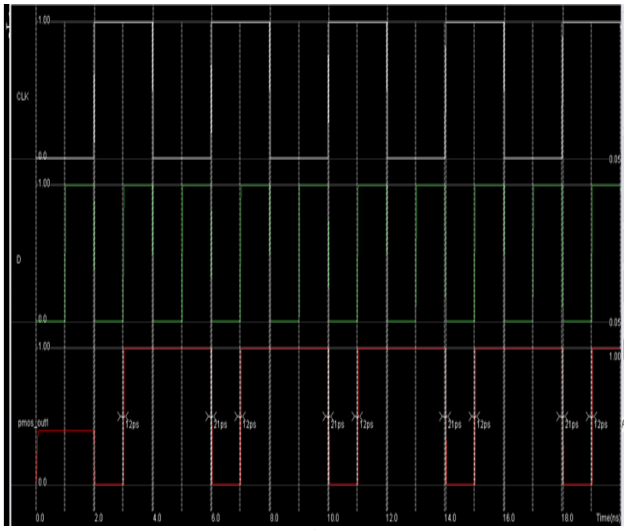

Fig.3: Simulation Output of TSPC based D Flip-Flop

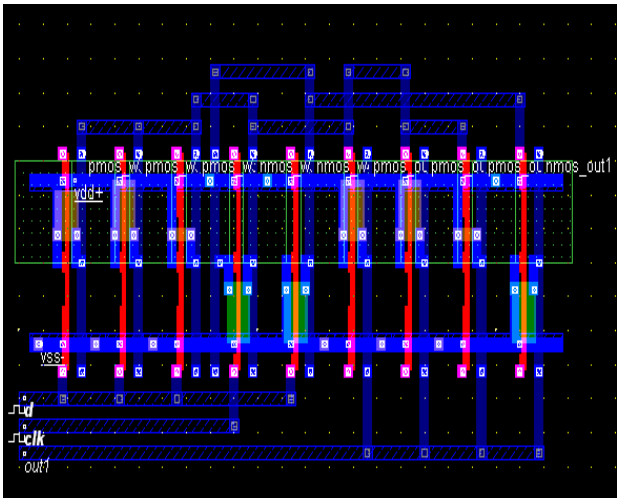

Fig.4: Layout of TSPC based D Flip-Flop

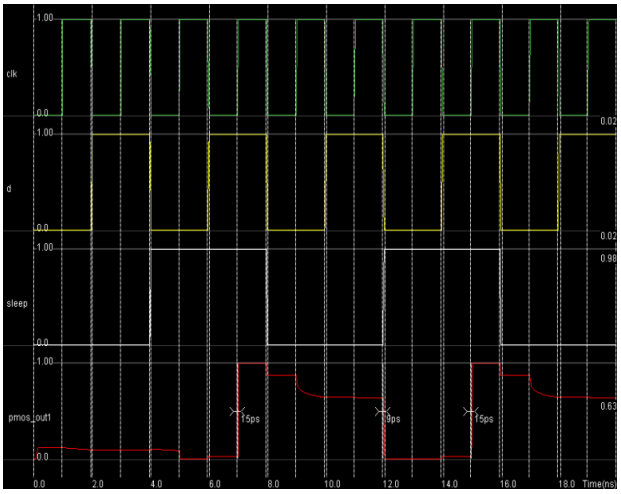

Fig.5: Simulation Output of MTCMOS based Flip-Flop

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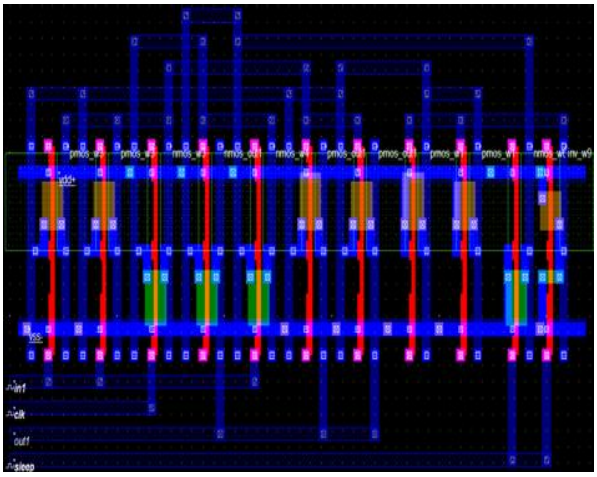

Fig.6: Layout of MTCMOS based D Flip-Flop

The comparison between different technologies and different scaled supply voltages is shown in Table.3 for TSPC based D Flip-Flop and Table.4 for MTCMOS based D Flip-Flop.

Table.3: power delay comparison for TSPC based D Flip-Flop

Parameters	90nm		70nm		50nm	
	0.5V	1V	0.5V	1V	0.5V	1V
Power Dissipation (µW)	2.01	2.853	2.57	3.10	2.853	4.01
Delay(nS)	0.126	0.137	0.134	0.094	0.137	0.069
Power Delay Product (fJ)	0.253	0.39	0.344	0.29	0.39	0.28

Table.4: Power Delay Comparison for MTCMOS based D Flip-Flop

Parameters	90nm		70nm		50nm	
	0.5 V	1V	0.5V	1V	0.5V	1V
Power Dissipation (µW)	0.514	1.97	0.473	1.837	0.280	1.173
Delay (nS)	0.142	0.142	0.236	0.23	0.370	0.236
Power Delay Product (fJ)	0.0729	0.28	0.111	0.42	0.104	0.277

From the tables 3 & 4 listed above, it is clear that the power dissipation decreases and propagation delay increases as the technology is scaled down. Also as the supply voltage is scaled down, both the power dissipation and propagation delay decrease. When compared with TSPC based D Flip-Flop, the MTCMOS based D Flip-Flop has advantage of low power delay product which is well suited for high performance applications.

4. CONCLUSION

This paper concludes that MTCMOS D Flip-Flop designed with 7 Transistors is having less power consumption. The Flip-Flops and latches are simulated for 90nm, 70nm and 50nm technology nodes using the DSCH and MICROWIND Tools. Hence from results, as the technology is scaled down power dissipation decreases and propagation delay increases. From the details of Figure of merit MTCMOS based Flip-Flop has least power delay product, which gives rise to best performance. Hence, the circuits designed using MTCMOS are suitable for high performance applications like level converters, microprocessors, clocking systems counters, etc.

5. REFERENCES

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