Xccela™ Flash Memory Data Sheet Brief

MT35X 1.8/3V, Octal I/O, 4KB/32KB/128KB Sector Erase

Features

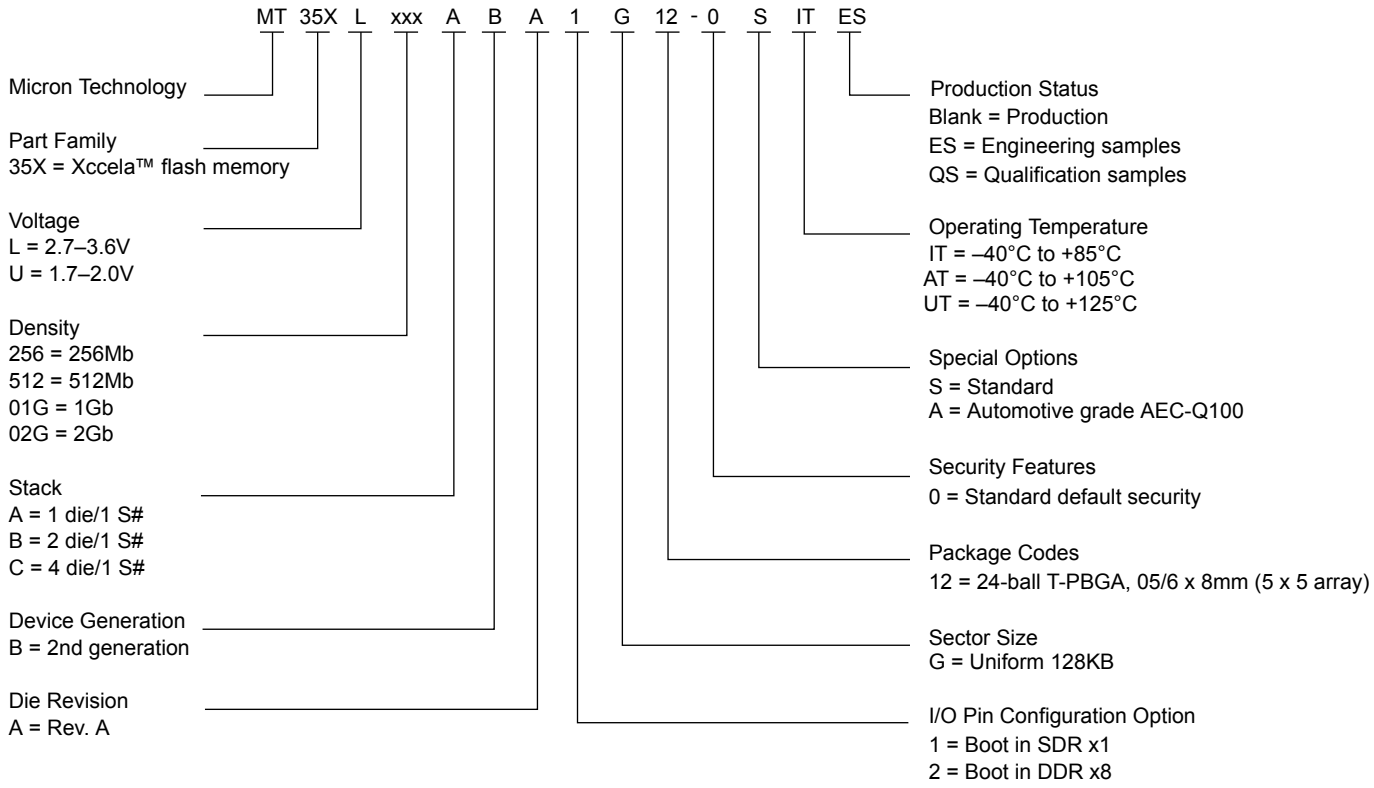
- SPI-compatible Xccela™ bus interface
  - Octal DDR protocol
  - Extended-SPI protocol with octal commands
- Single and double transfer rate (SDR/DDR)
- Clock frequency:
  - 166 MHz (MAX) SDR; 166 MB/s (1.8V)
  - 200 MHz (MAX) DDR; 400 MB/s with DQS (1.8V)
  - 133 MHz (MAX) SDR; 133 MB/s (3.0V)
  - 133 MHz (MAX) DDR; 266MB/s with DQS (3.0V)
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Reset pin available
- 3-byte and 4-byte address modes – enable memory access beyond 128Mb
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Bulk erase for monolithic, die erase for stacked devices
  - Sector erase 128KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 128KB sector
  - Nonvolatile configuration locking and password protection
  - Protection management register offering enhanced security features
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature
  - Extended device ID: two additional bytes identify device factory options
- JESD47I-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 1.7–2.0V	U
– 2.7–3.6V	L
• Density	
– 256Mb	256
– 512Mb	512
– 1Gb	01G
– 2Gb	02G
• Device stacking	
– Monolithic	A
– 2 die stacked	B
– 4 die stacked	C
• Device Generation	B
• Die revision	A
• Configuration	
– Boot in SDR x1	1
– Boot in DDR x8	2
• Sector Size	
– 128KB	G
• Packages: JEDEC-standard, RoHS-compliant	
– 24-ball T-PBGA 05/6mm x 8mm (5 x 5 array)	12
• Security features	
– Standard security	0
• Special options	
– Standard	S
– Automotive	A
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT
– From –40°C to +125°C	UT

Part Number Ordering

Micron® Xccela flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information



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Device Description

This data sheet brief enables the development of the MT35X software driver. For further MT35X information, please refer to the complete MT35X data sheet, for which an NDA is required.

Note: For the complete MT35X data sheet, please contact your sales representative.

The Micron Xccela flash is a high-performance, multiple I/O, SPI-compatible flash memory device. It features a high-speed, low pin count Xccela bus interface with a DDR clock frequency of up to 200 MHz for 1.8V parts and up to 133 MHz for 3.0 V parts, using eight I/O signals and a data strobe (DQS pin).

SUSPEND and RESUME commands provide the ability to pause and resume PROGRAM/ERASE operations. Nonvolatile and volatile configuration registers enable respective default and temporary settings such as READ operation dummy clock cycles and wrap modes, memory protection, output buffer impedance, SPI protocol type and XIP mode.

Memory is organized as uniform 128KB sectors, 4KB and 32KB subsectors, and 256 byte pages. The device also includes a 64-byte one-time-programmable (OTP) memory area that can be permanently locked.

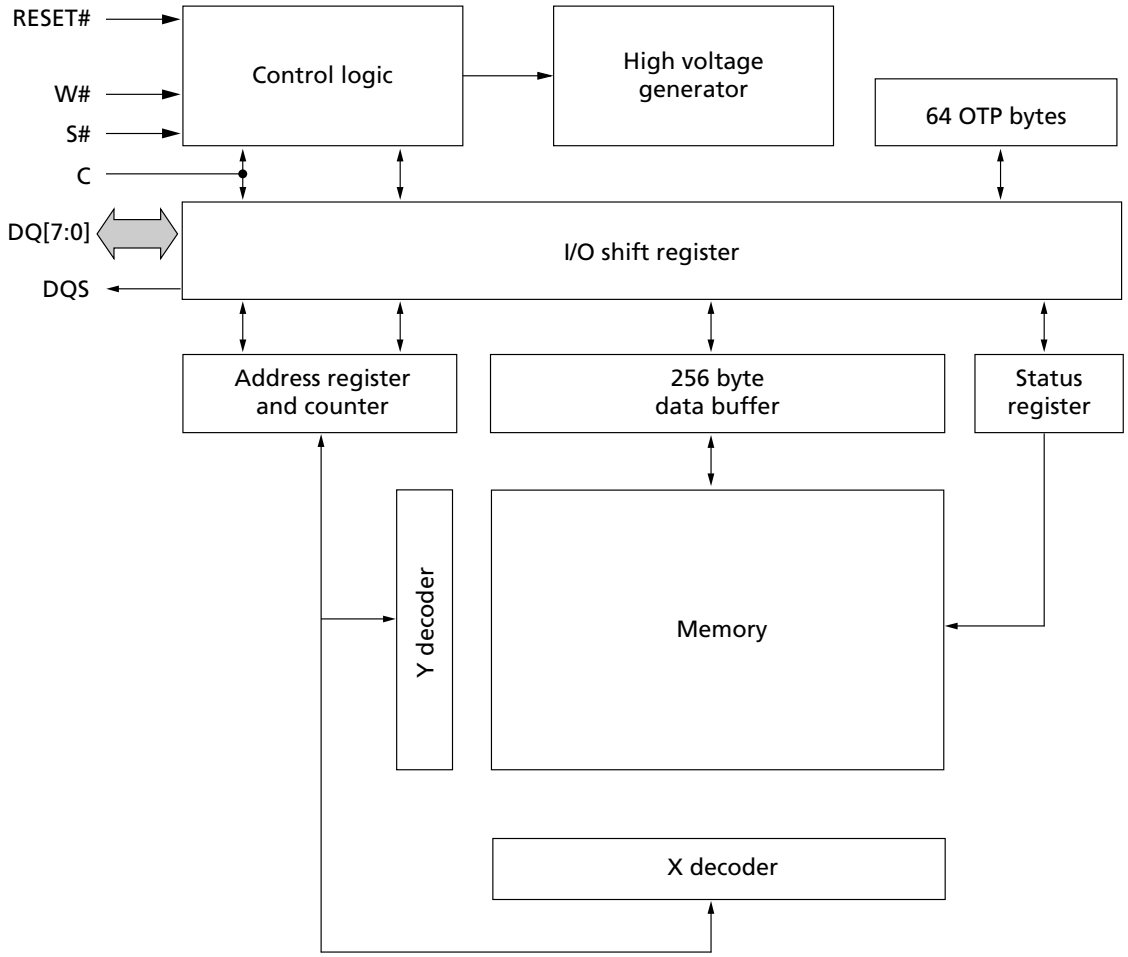
Direct boot in octal DDR protocol provides high performance and ease of use, enabling communication between the host and flash device without need to configure extended SPI protocol operations. However, the device still supports both extended SPI and octal DDR protocols to ensure legacy system support and an easy migration path. The extended SPI protocol supports address and data transmission on one or eight data lines, depending on the command.

Information in octal DDR protocol is always transmitted by eight data lines on both rising and falling clock edges. Most legacy x1 SPI commands are supported, but require only one clock cycle because the command is latched on both the rising and falling edges of the clock. Address cycles are fixed at 4-byte READ operations from the flash array.

The host is not required to drive DQS during the input operation to the memory. The data input (DQ) to the memory still relies on clock (C) to latch all address and data operations. Most register outputs require dummy clock cycles due to the critical timing from command decoding. With the help of DQS for data latching, the number of dummy clocks is transparent to the host.

Block Diagram

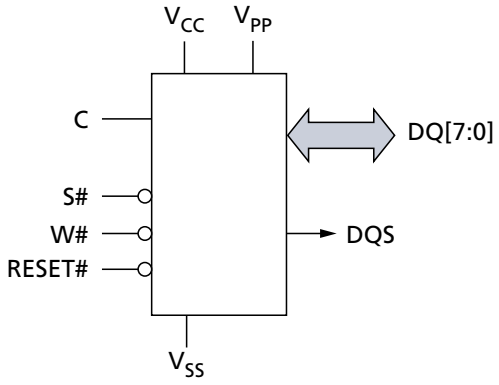
Figure 2: Block Diagram – Components and Signals



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

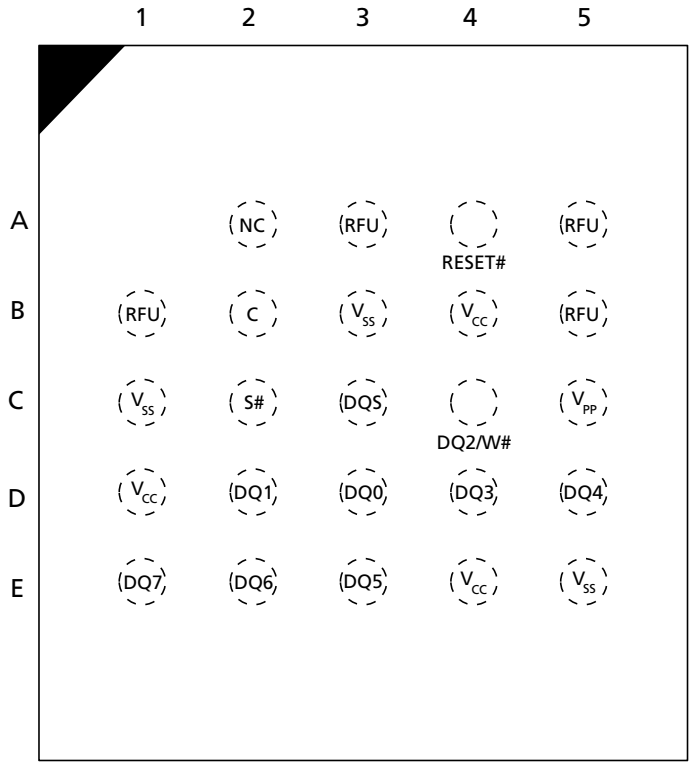
Device Logic Diagram

Figure 3: Logic Diagram



Signal Assignments

Figure 4: 24-Ball TBGA, 5 x 5 (Balls Down)



Signal Descriptions

The table below is a comprehensive list of device signals. All signals listed may not be supported. See Signal Assignments for device-specific information.

Table 1: Signal Descriptions

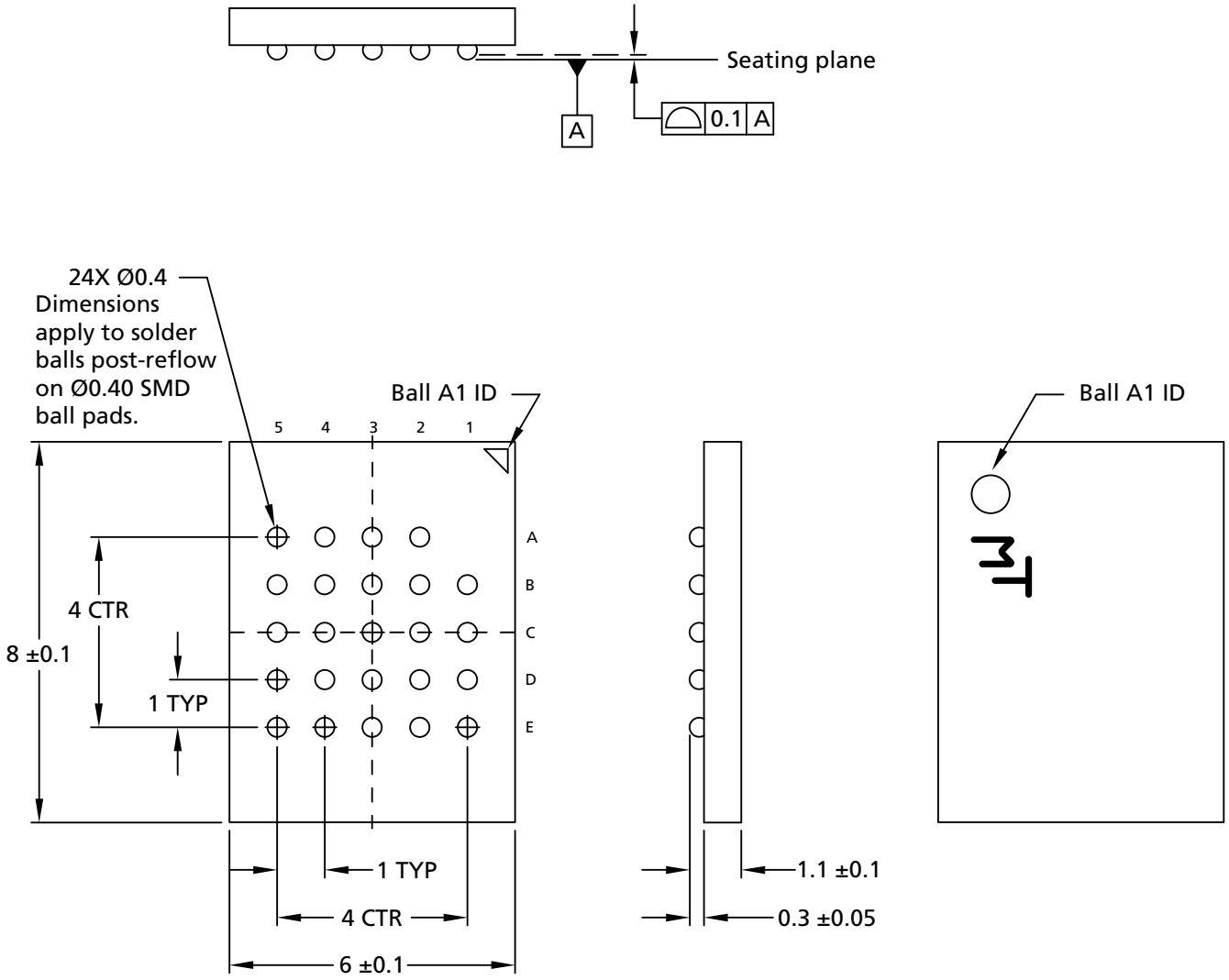
Symbol	Type	Description
C	Input	**Clock:** Provides timing for the serial interface. Command, address, or data inputs are latched on the rising edge of C. Data is shifted out on the falling edge of C.
S#	Input	**Chip select:** When S# is LOW, device is selected and in active power mode. Operations are initiated on the falling edge of S#. When S# is HIGH, device is deselected, DQ pins are tri-stated, and unless an internal WRITE operation is in progress, device enters standby mode.
RESET#	Input	**RESET:** Resets device to its default settings, such as after a volatile configuration register setting which then requires a return to the device default setting. Reset is optional when device settings are fixed by nonvolatile configuration register settings and always synchronized with the host. This pad is internally tied to weak pull-up so the pin can be floated.
W#	Input	**Write protect:** This input signal is used to freeze the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not be executed. During the extended-SPI protocol with OCTAL READ/PROGRAM instructions, and during octal DDR protocol, this pin functions are an input/output (DQ2 functionality). This signal does not have internal pull-ups, it should not be left floated and must be driven, even if none of W#/DQ2 function is used.
CP	Input	**Phase-shifted serial clock:**This input signal provides the timing for data strobe signal. It is a 90 degree phase shifted signal from serial clock (C), and the DQS output will be generated based on this input, and is always centered for all the DQ outputs, so on the host end the DQ outputs can be directly latched by the DQS output. CP is only enabled on dedicated product line item.
DQ[7:0]	I/O	**Serial I/O:** Bidirectional signals that transfer address, data, and command information. In extended-SPI protocol, DQ0 functions as input and DQ1 as output. DQ[7:2] are not used. In octal protocol, input/output on DQ[7:0] depends on the command. Input can be latched on the rising edge of C (SDR) or on both edges of C (DDR). Data can be shifted out on the falling edge of C (SDR) or on both edges of C (DDR). In octal DDR, DQ[7:0] always function as I/O, input is latched on both edges of C, and output is shifted out on both edges of C. DQ2 is used also as write protection control.
DQS	Output	**Data strobe:** Indicates output data valid for DDR modes and is required to support high speed data output. Not required in extended-SPI protocol except to achieve high frequency for specific DDR commands. Used for READ but not for WRITE operations. Configured by nonvolatile and volatile configuration register bit 5 at address 00h. When enabled, DQS is driven to ground at S# LOW and until the device is driving output data, in which case DQS toggles to synchronize data output. When not enabled, DQS is not driven.
V_{CC}	Supply	**Supply voltage:** Core and I/O supply.
V_{PP}	Supply	**Supply voltage:** If V_{PP} is in the voltage range of V_{PPH}, the signal acts as an additional power supply for programming operation, as defined in the Operating Conditions table. The V_{PP} pad will be internally pulled up to V_{CC}, so customer can leave V_{PP} pin floated if not used.
V_{SS}	Supply	**Ground:** Core and I/O ground connection. V_{SS} is the reference for the V_{CC} supply voltage.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
DNU	–	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
RFU	–	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. Recommend that these should be left floating. May be connected internally, but external connections will not affect operation.
NC	–	**No connect :** No internal connection; can be driven or floated.

Package Dimensions – Package Code: 12

Figure 5: 24-Ball T-PBGA (5 x 5 ball grid array) – 6mm x 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Volatile Configuration Register

Volatile configuration register bits temporarily set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme; however, only the LSB is used to access different register settings to provide up to 256 bytes of registers (See the table below for the details). A READ command from a reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit is cleared.

Table 2: Volatile Configuration Register

Address	Name	Settings	Description	Notes
255h:08h	Reserved	Reserved	Reserved	
07h	Wrap configuration	FFh = Continuous (Default) FEh = 64-byte wrap FDh = 32-byte wrap FCh = 16-byte wrap Others = Reserved	Enables the device to read from memory sequentially or to wrap within 16-, 32-, or 64-byte boundaries.	
06h	XIP configuration	FFh = XIP disabled (Default) FEh = XIP enabled Others = Reserved	Enables the device to operate in the selected XIP mode. It is first required to enable XiP and then enter XIP mode using the XiP confirmation bit.	
05h	Beyond 128Mb address configuration	FFh = 3-byte address (Default) FEh = 4-byte address Others = Reserved	Defines the number of address bytes for a command.	
04h	Reserved	Reserved	Reserved	
03h	Programmable output drive strength	FFh = 50Ω (Default) FEh = 35Ω FDh = 25Ω FCh = 18Ω Others = Reserved	Optimizes the impedance at V_{CC}/2 output voltage.	
02h	Reserved	Reserved	Reserved	
01h	Dummy cycle configuration	00h = Identical to 1Fh 01h = 1 dummy cycle 02h = 2 dummy cycles 03h to 1Dh = 3 to 29 dummy cycles 1Eh = 30 dummy cycles 1Fh = Default Others = Reserved	Sets the number of dummy clock cycles subsequent to all FAST READ commands (See the Command Set Table for default setting values).	1

Table 2: Volatile Configuration Register (Continued)

Address	Name	Settings	Description	Notes
00h	I/O mode	FFh = Extended SPI (Default) DFh = Extended SPI without DQS E7h = Octal DDR C7h = Octal DDR without DQS Others = Reserved	Sets the device to work in different I/O modes such as DDR mode or DQS mode (strobe enabled).	

Note: 1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command. Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.

Device ID Data

The device ID data shown in the tables here is read by the READ ID and MULTIPLE I/O READ ID operations.

Table 3: Device ID Data

Byte#	Name	Content Value	Assigned By
Manufacturer ID (1 Byte total)			
1	Manufacturer ID (1 Byte)	2Ch	JEDEC
Device ID (2 bytes total)			
2	Memory type (1 Byte)	5Ah = 3V	Manufacturer
		5Bh = 1.8V	
3	Memory capacity (1 byte)	1Ch = 2Gb	
		1Bh = 1Gb	
		1Ah = 512Mb	
		19h = 256Mb	
Unique ID (17 bytes total)			
4	Indicates the number of remaining ID bytes (1 byte)	10h	Factory
5	Extended device ID (1 byte)	See Extended Device ID table	
6	Device configuration information (1 byte)	See Device Configuration Information table	
7:20	Customized factory data (14 bytes)	Unique ID code (UID)	

Table 4: Extended Device ID Data, First Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Device generation 1 = 2nd generation	Reserved	Reserved	Reserved	Reserved	Sector size: 01 = Uniform 128KB	

Table 5: Device Configuration Information Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Boot up protocol: 0 = Boot in SDR ×1 1 = Boot in DDR ×8	Reserved	

Serial Flash Data Parameter – Header Structure

The table below shows the MT35X family SFDP data. Data in these tables is read by the READ SERIAL FLASH DISCOVERY PARAMETER operation (5Ah).

Table 6: SFDP Header Structure

Description		Byte Address	Bits	Data			
				256Mb	512Mb	1Gb	2Gb
SFDP signature		00h	7:0	53h	53h	53h	53h
		01h	7:0	46h	46h	46h	46h
		02h	7:0	44h	44h	44h	44h
		03h	7:0	50h	50h	50h	50h
Parameter revision	Minor	04h	7:0	06h	06h	06h	06h
	Major	05h	7:0	01h	01h	01h	01h
Number of parameter headers		06h	7:0	01h	01h	01h	01h
Unused		07h	7:0	FFh	FFh	FFh	FFh
Parameter 0 ID LSB		08h	7:0	00h	00h	00h	00h
Parameter revision	Minor	09h	7:0	06h	06h	06h	06h
	Major	0Ah	7:0	01h	01h	01h	01h
Parameter length in data words (DW)		0Bh	7:0	10h	10h	10h	10h
Parameter table pointer		0Ch	7:0	30h	30h	30h	30h
		0Dh	7:0	00h	00h	00h	00h
		0Eh	7:0	00h	00h	00h	00h
Parameter 1 ID most significant bit (MSB)		0Fh	7:0	FFh	FFh	FFh	FFh
Parameter 2 ID least significant bit (LSB)		10h	7:0	84h	84h	84h	84h
Parameter revision	Minor	11h	7:0	00h	00h	00h	00h
	Major	12h	7:0	01h	01h	01h	01h
Parameter length in DW		13h	7:0	02h	02h	02h	02h
Parameter table pointer		14h	7:0	80h	80h	80h	80h
		15h	7:0	00h	00h	00h	00h
		16h	7:0	00h	00h	00h	00h
Parameter 2 ID MSB		17h	7:0	FFh	FFh	FFh	FFh

Note: 1. Locations from 18h to 2Fh contain FFh.

Serial Flash Data Parameter – Basic Properties

Table 7: Parameter Table – Flash Basic Properties

Description	Byte Address	Bits	Data			
			256Mb	512Mb	1Gb	2Gb
Minimum sector erase sizes	30h	1:0	01b	01b	01b	01b
Write granularity		2	1	1	1	1
WRITE ENABLE command required for writing to volatile status registers		3	0	0	0	0
WRITE ENABLE command selected for writing to volatile status registers		4	0	0	0	0
Not used		7:5	111b	111b	111b	111b
4KB ERASE command	31h	7:0	20h	20h	20h	20h
Supports 1-1-2 FAST READ	32h	0	0	0	0	0
Address bytes		2:1	01b	01b	01b	01b
Supports double transfer rate clocking		3	1	1	1	1
Supports 1-2-2 FAST READ		4	0	0	0	0
Supports 1-4-4 FAST READ		5	0	0	0	0
Supports 1-1-4 FAST READ		6	0	0	0	0
Not used		7	1	1	1	1
Reserved	33h	7:0	FFh	FFh	FFh	FFh
Flash size (bits)	34h	7:0	FFh	FFh	FFh	FFh
	35h	7:0	FFh	FFh	FFh	FFh
	36h	7:0	FFh	FFh	FFh	FFh
	37h	7:0	0Fh	1Fh	3Fh	7Fh
1-4-4 FAST READ dummy cycle count	38h	4:0	00000b	00000b	00000b	00000b
1-4-4 FAST READ number of mode bits		7:5	000b	000b	000b	000b
1-4-4 FAST READ command code	39h	7:0	00h	00h	00h	00h
1-1-4 FAST READ dummy cycle count	3Ah	4:0	00000b	00000b	00000b	00000b
1-1-4 FAST READ number of mode bits		7:5	000b	000b	000b	000b
1-1-4 FAST READ command code	3Bh	7:0	00h	00h	00h	00h
1-1-2 FAST READ dummy cycle count	3Ch	4:0	00000b	00000b	00000b	00000b
1-1-2 FAST READ number of mode bits		7:5	000b	000b	000b	000b
1-1-2 FAST READ command	3Dh	7:0	00h	00h	00h	00h

Table 7: Parameter Table – Flash Basic Properties (Continued)

Description	Byte Address	Bits	Data			
			256Mb	512Mb	1Gb	2Gb
1-2-2 FAST READ dummy cycle count	3Eh	4:0	00000b	00000b	00000b	00000b
1-2-2 FAST READ number of mode bits		7:5	000b	000b	000b	000b
1-2-2 Command code	3Fh	7:0	00h	00h	00h	00h
Supports 2-2-2 FAST READ	40h	0	0	0	0	0
Reserved		3:1	111b	111b	111b	111b
Supports 4-4-4 FAST READ		4	0	0	0	0
Reserved		7:5	111b	111b	111b	111b
Reserved	43:41h	31:8	FFFFFFh	FFFFFFh	FFFFFFh	FFFFFFh
Reserved	45:44h	15:0	FFFFh	FFFFh	FFFFh	FFFFh
2-2-2 FAST READ dummy cycle count	46h	4:0	00000b	00000b	00000b	00000b
2-2-2 FAST READ number of mode bits		7:5	000b	000b	000b	000b
2-2-2 FAST READ command code	47h	7:0	00h	00h	00h	00h
Reserved	49:48h	15:0	FFFFh	FFFFh	FFFFh	FFFFh
4-4-4 FAST READ dummy cycle count	4Ah	4:0	00000b	00000b	00000b	00000b
4-4-4 FAST READ number of mode bits		7:5	000b	000b	000b	000b
4-4-4 FAST READ command code	4Bh	7:0	00h	00h	00h	00h
Sector Type 1 size	4Ch	7:0	0Ch	0Ch	0Ch	0Ch
Sector Type 1 command code	4Dh	7:0	20h	20h	20h	20h
Sector Type 2 size	4Eh	7:0	11h	11h	11h	11h
Sector Type 2 code	4Fh	7:0	D8h	D8h	D8h	D8h
Sector Type 3 size	50h	7:0	0Fh	0Fh	0Fh	0Fh
Sector Type 3 code	51h	7:0	52h	52h	52h	52h
Sector Type 4 size	52h	7:0	00h	00h	00h	00h
Sector Type 4 code	53h	7:0	00h	00h	00h	00h
Multiplier from typical erase time to maximum erase time	57h:54h	3:0	0100b	0100b	0100b	0100b
Sector Type 1 ERASE time (TYP)		8:4	00010b	00010b	00010b	00010b
		10:9	01b	01b	01b	01b
Sector Type 2 ERASE time (TYP)		15:11	01011b	01011b	01011b	01011b
		17:16	01b	01b	01b	01b
Sector Type 3 ERASE time (TYP)		22:18	00110b	00110b	00110b	00110b
		24:23	01b	01b	01b	01b
Sector Type 4 ERASE time (TYP)		29:25	00000b	00000b	00000b	00000b
		31:30	00b	00b	00b	00b

Table 7: Parameter Table – Flash Basic Properties (Continued)

Description	Byte Address	Bits	Data			
			256Mb	512Mb	1Gb	2Gb
Multiplier from typical time to maximum time for page or byte PROGRAM	5Bh:58h	3:0	1011b	1011b	1011b	1011b
Page size		7:4	1000b	1000b	1000b	1000b
Page PROGRAM time (TYP)		12:8	01110b	01110b	01110b	01110b
		13	0b	0b	0b	0b
Page PROGRAM time, first byte (TYP)		17:14	1110b	1110b	1110b	1110b
		18	0b	0b	0b	0b
Byte PROGRAM time, additional byte (TYP)[1]		22:19	0000b	0000b	0000b	0000b
		23[1]	0b	0b	0b	0b
Chip ERASE time (TYP)		28:24	00000b	00001b	00001b	00001b
		30:29	11b	11b	11b	11b
Reserved		31	1b	1b	1b	1b
Prohibited operations during PROGRAM SUSPEND	5Fh:5Ch	3:0	1100b	1100b	1100b	1100b
Prohibited operations during ERASE SUSPEND		7:4	1010b	1010b	1010b	1010b
Reserved		8	1b	1b	1b	1b
PROGRAM RESUME to SUSPEND interval[2]		12:9[2]	0000b	0000b	0000b	0000b
SUSPEND in progress program maximum latency		17:13	11000b	11000b	11000b	11000b
		19:18	01b	01b	01b	01b
ERASE RESUME to SUSPEND interval		23:20	0010b	0010b	0010b	0010b
SUSPEND in progress erase maximum latency		28:24	11000b	11000b	11000b	11000b
		30:29	01b	01b	01b	01b
SUSPEND RESUME supported		31	0b	0b	0b	0b
PROGRAM RESUME command	60h	7:0	7Ah	7Ah	7Ah	7Ah
PROGRAM SUSPEND command	61h	7:0	75h	75h	75h	75h
RESUME command	62h	7:0	7Ah	7Ah	7Ah	7Ah
SUSPEND command	63h	7:0	75h	75h	75h	75h

Table 7: Parameter Table – Flash Basic Properties (Continued)

Description	Byte Address	Bits	Data			
			256Mb	512Mb	1Gb	2Gb
Reserved	67h:64h	1:0	11b	11b	11b	11b
Status register polling device busy		2	0b	0b	0b	0b
		3	1b	1b	1b	1b
		7:4	1111b	1111b	1111b	1111b
EXIT DEEP POWER-DOWN to next operation delay		12:8	11101b	11101b	11101b	11101b
		14:13	01b	01b	01b	01b
EXIT DEEP POWER-DOWN command		22:15	ABh	ABh	ABh	ABh
ENTER DEEP POWER-DOWN command		30:23	B9h	B9h	B9h	B9h
Deep power-down supported		31	0b	0b	0b	0b
4-4-4 mode disable sequence	6Bh:68h	3:0	0000b	0000b	0000b	0000b
4-4-4 mode enable sequence		8:4	0_0000b	0_0000b	0_0000b	0_0000b
0-4-4 mode supported		9	0b	0b	0b	0b
0-4-4 mode exit method		15:10	00_0000b	00_0000b	00_0000b	00_0000b
0-4-4 mode entry method		19:16	0000b	0000b	0000b	0000b
Quad enable requirements		22:20	111b	111b	111b	111b
HOLD and WP disable		23	0b	0b	0b	0b
Reserved		31:24	FFh	FFh	FFh	FFh
Volatile and nonvolatile register and WRITE ENABLE	6Fh: 6Ch	6:0	0000001b	0000001b	0000001b	0000001b
Reserved		7	1b	1b	1b	1b
Soft reset and rescue sequence support		13:8	110000b	110000b	110000b	110000b
EXIT 4-BYTE ADDRESS		23:14	00_1110_0010b	00_1110_0010b	00_1110_0010b	00_1110_0010b
ENTER 4-BYTE ADDRESS		31:24	0011_0110b	0011_0110b	0011_0110b	0010_0010b

Notes:
1. Per industry standards, 1µs is the minimum allowed.
2. Per industry standards, 64µs is the minimum allowed.
3. Locations from 70h to 7Fh contain FFh.

Serial Flash Data Parameter – 4-Byte Address Command

Table 8: Parameter Table – 4-Byte Address Command

Description	Byte Address	Bits	Data			
			256Mb	512Mb	1Gb	2Gb
4-Byte Address Instruction Table DW1	80h	0	1b	1b	1b	1b
		1	1b	1b	1b	1b
		2	0b	0b	0b	0b
		3	0b	0b	0b	0b
		4	0b	0b	0b	0b
		5	0b	0b	0b	0b
		6	1b	1b	1b	1b
		7	0b	0b	0b	0b
	81h	0	0b	0b	0b	0b
		1	1b	1b	1b	1b
		2	1b	1b	1b	1b
		3	1b	1b	1b	1b
		4	0b	0b	0b	0b
		5	0b	0b	0b	0b
		6	0b	0b	0b	0b
		7	0b	0b	0b	0b
	82h	0	1b	1b	1b	1b
		1	1b	1b	1b	1b
		2	1b	1b	1b	1b
		3	1b	1b	1b	1b
		7:4	1111b	1111b	1111b	1111b
	83h	7:0	FFh	FFh	FFh	FFh
4-Byte Address Instruction Table DW2	84h	7:0	21h	21h	21h	21h
	85h	7:0	DCh	DCh	DCh	DCh
	86h	7:0	5Ch	5Ch	5Ch	5Ch
	87h	7:0	FFh	FFh	FFh	FFh

Note: 1. Locations from 88h and above contain FFh.

Command Definitions

Table 9: Command Set

Command	Code	Extended SPI		Octal SPI		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
Software RESET Operations							
RESET ENABLE	66h	1-0-0	0	8-0-0	0	0	0
RESET MEMORY	99h	1-0-0	0	8-0-0	0	0	0
READ ID Operations							
READ ID	9E/9Fh	1-0-1	0	8-0-8	8	0	1 to 20
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	1-1-1	8	8-8-8	8	3[1]	1 to ∞
READ MEMORY Operations							
READ	03h	1-1-1	0	–	–	3[2]	1 to ∞
FAST READ	0Bh	1-1-1	8	8-8-8	16	3[2]	1 to ∞
OCTAL OUTPUT FAST READ	8Bh	1-1-8	8	8-8-8	16	3[2]	1 to ∞
OCTAL I/O FAST READ	CBh	1-8-8	16	8-8-8	16	3[2]	1 to ∞
DDR OCTAL OUTPUT FAST READ	9Dh	1-1-8	8	8-8-8	16	3[2]	1 to ∞
DDR OCTAL I/O FAST READ	FDh	1-8-8	16	8-8-8	16	4	1 to ∞
READ MEMORY Operations with 4-Byte Address							
4-BYTE READ	13h	1-1-1	0	–	–	4	1 to ∞
4-BYTE FAST READ	0Ch	1-1-1	8	8-8-8	16	4	1 to ∞
4-BYTE OCTAL OUTPUT FAST READ	7Ch	1-1-8	8	8-8-8	16	4	1 to ∞
4-BYTE OCTAL I/O FAST READ	CCh	1-8-8	16	8-8-8	16	4	1 to ∞
WRITE Operations							
WRITE ENABLE	06h	1-0-0	0	8-0-0	0	0	0
WRITE DISABLE	04h	1-0-0	0	8-0-0	0	0	0
READ REGISTER Operations							
READ STATUS REGISTER	05h	1-0-1	0	8-0-8	8	0	1 to ∞
READ FLAG STATUS REGISTER	70h	1-0-1	0	8-0-8	8	0	1 to ∞
READ NONVOLATILE CONFIGURATION REGISTER	B5h	1-1-1	8	8-8-8	8	3[2]	1 to ∞
READ VOLATILE CONFIGURATION REGISTER	85h	1-1-1	8	8-8-8	8	3[2]	1 to ∞
READ PROTECTION MANAGEMENT REGISTER	2Bh	1-0-1	0	8-0-8	8	0	1 to ∞
READ GENERAL PURPOSE READ REGISTER	96h[3, 4]	1-0-1	8	8-0-8	8	0	1 to ∞

Table 9: Command Set (Continued)

Command	Code	Extended SPI		Octal SPI		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
WRITE REGISTER Operations							
WRITE STATUS REGISTER	01h	1-0-1	0	8-0-8	0	0	1
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	1-1-1	0	8-8-8	0	3[2]	1
WRITE VOLATILE CONFIGURATION REGISTER	81h	1-1-1	0	8-8-8	0	3[2]	1
WRITE PROTECTION MANAGEMENT REGISTER	68h	1-0-1	0	8-0-8	0	0	1
CLEAR FLAG STATUS REGISTER Operation							
CLEAR FLAG STATUS REGISTER	50h	1-0-0	0	8-0-0	0	0	0
PROGRAM Operations							
PAGE PROGRAM	02h	1-1-1	0	8-8-8	0	3[2]	1 to 256
OCTAL INPUT FAST PROGRAM	82h	1-1-8	0	8-8-8	0	3[2]	1 to 256
EXTENDED OCTAL INPUT FAST PROGRAM	C2h	1-8-8	0	8-8-8	0	3[2]	1 to 256
PROGRAM Operations with 4-Byte Address							
4-BYTE PAGE PROGRAM	12h	1-1-1	0	8-8-8	0	4	1 to 256
4-BYTE OCTAL INPUT FAST PROGRAM	84h	1-1-8	0	8-8-8	0	4	1 to 256
4-BYTE OCTAL INPUT EXTENDED FAST PROGRAM	8Eh	1-8-8	0	8-8-8	0	4	1 to 256
ERASE Operations							
32KB SUBSECTOR ERASE	52h	1-1-0	0	8-8-0	0	3[2]	0
4KB SUBSECTOR ERASE	20h	1-1-0	0	8-8-0	0	3[2]	0
SECTOR ERASE	D8h	1-1-0	0	8-8-0	0	3[2]	0
BULK ERASE[6]	C7h/60h	1-0-0	0	8-0-0	0	0	0
DIE ERASE[7]	C4h	1-1-0	0	8-8-0	0	32	0
ERASE Operations with 4-Byte Address							
4-BYTE SECTOR ERASE	DCh	1-1-0	0	8-8-0	0	4	0
4-BYTE 4KB SUBSECTOR ERASE	21h	1-1-0	0	8-8-0	0	4	0
4-BYTE 32KB SUBSECTOR ERASE	5Ch	1-1-0	0	8-8-0	0	4	0
SUSPEND/RESUME Operations							
PROGRAM/ERASE SUSPEND	75h	1-0-0	0	8-0-0	0	0	0
PROGRAM/ERASE RESUME	7Ah	1-0-0	0	8-0-0	0	0	0
ONE-TIME PROGRAMMABLE (OTP) Operations							

Table 9: Command Set (Continued)

Command	Code	Extended SPI		Octal SPI		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
READ OTP ARRAY	4Bh	1-1-1	8	8-8-8	16	3[2]	1 to 65
PROGRAM OTP ARRAY	42h	1-1-1	0	8-8-8	0	3[2]	1 to 65
4-BYTE ADDRESS MODE Operations							
ENTER 4-BYTE ADDRESS MODE	B7h	1-0-0	0	8-0-0	0	0	0
EXIT 4-BYTE ADDRESS MODE	E9h	1-0-0	0	8-0-0	0	0	0
DEEP POWER-DOWN Operations							
ENTER DEEP POWER-DOWN	B9h	1-0-0	0	8-0-0	0	0	0
RELEASE FROM DEEP POWER-DOWN	ABh	1-0-0	0	8-0-0	0	0	0
ADVANCED SECTOR PROTECTION Operations							
READ SECTOR PROTECTION	2Dh	1-0-1	0	8-0-8	8	0	1 to ∞
PROGRAM SECTOR PROTECTION	2Ch	1-0-1	0	8-0-8	0	0	2
READ VOLATILE LOCK BITS	E8h	1-1-1	0	8-8-8	8	3[2]	1 to ∞
WRITE VOLATILE LOCK BITS	E5h	1-1-1	0	8-8-8	0	3[2]	1
READ NONVOLATILE LOCK BITS	E2h	1-1-1	0	8-8-8	8	4	1 to ∞
WRITE NONVOLATILE LOCK BITS	E3h	1-1-0	0	8-8-0	0	4	0
ERASE NONVOLATILE LOCK BITS	E4h	1-0-0	0	8-0-0	0	0	0
READ GLOBAL FREEZE BIT	A7h	1-0-1	0	8-0-8	8	0	1 to ∞
WRITE GLOBAL FREEZE BIT	A6h	1-0-0	0	8-0-0	0	0	0
READ PASSWORD	27h[5]	1-0-1	0	8-0-8	8	0	1 to ∞
WRITE PASSWORD	28h	1-0-1	0	8-0-8	0	0	8
UNLOCK PASSWORD	29h	1-0-1	0	8-0-8	0	0	8
ADVANCED SECTOR PROTECTION Operations with 4-Byte Address							
4-BYTE READ VOLATILE LOCK BITS	E0h	1-1-1	0	8-8-8	8	4	1 to ∞
4-BYTE WRITE VOLATILE LOCK BITS	E1h	1-1-1	0	8-8-8	0	4	1
ADVANCED FUNCTION INTERFACE Operations							
CYCLIC REDUNDANCY CHECK	9Bh/27h	1-0-1	0	8-0-8	0	0	10 or 18

Notes: 1. Read SFDP instruction accepts only 3-byte address even if the device is configured to 4-byte address mode. In octal DDR mode, it will be fixed 4-byte address cycle. The number of dummy cycles for the READ SFDP command is fixed (8 dummy cycles) and is not affected by dummy cycle settings in the nonvolatile configuration register and volatile con-

figuration register. For the max clock frequency achievable refer to Supported Clock Frequencies tables for 8 dummy cycles.

2. Requires 4 bytes of address if the device is configured to 4-byte address mode or octal DDR protocol.
3. The number of dummy cycles for the READ GENERAL PURPOSE READ REGISTER command is fixed (8 dummy cycles) and is not affected by dummy cycle settings in the nonvolatile configuration register and volatile configuration register.
4. The general purpose read register is 64 bytes. After the first 64 bytes, the device outputs wrap.
5. After the 8-bit instruction shifted in, the 64-bit data are shifted out, the least significant byte first, most significant bit of each byte first. The READ PASSWORD instruction is terminated by driving chip select (S#) HIGH at any time during data output. When read continuously, the device outputs the 64-bit data repeatedly.
6. BULK ERASE command is applicable to 256Mb and 512Mb only.
7. DIE ERASE command is applicable to 1Gb and 2Gb only.

Revision History

Rev. A – 10/18

- Initial release

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.